

File 2:INSPEC 1969-2000/Mar W4  
(c) 2000 Institution of Electrical Engineers  
S1 840 CI=AL (S)CI=TI(S)CI=CU  
S3 44034 INTERCONNECTION?  
S4 31 S1 AND S2 5,7,8,15,18,19,20,21,26

?t /3,ab,ci/5,7,8,15,18,19,20,21,26

4/3,AB,CI/5

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

5194849 INSPEC Abstract Number: A9606-6822-022, B9604-2550F-025

**Title: Segregation of Si and Cu at AlSiCu/TiN interfaces**

Author(s): Kameyama, A.; Yaoita, A.; Kitano, T.; Saito, S.

Author Affiliation: ULSI Device Dev. Lab., NEC Corp., Sagamihara, Japan

Conference Title: Structure and Properties of Multilayered Thin Films.

Symposium p.407-12

Editor(s): Nguyen, T.D.; Lairson, B.M.; Clemens, B.M.; Shin, S.-C.; Sato, K.

Publisher: Mater. Res. Soc, Pittsburgh, PA, USA

Publication Date: 1995 Country of Publication: USA xii+496 pp.

Material Identity Number: XX96-00173

Conference Title: Structure and Properties of Multilayered Thin Films.

Symposium

Conference Date: 17-20 April 1995 Conference Location: San Francisco, CA, USA

Language: English

Abstract: The behavior of Cu and Si in the Al-alloy/TiN interface has been demonstrated by techniques of SIMS, GDS, XRD and AES. Cu and Si were observed to segregate at the AlSiCu/TiN interfaces just after sputtering. This segregation occurred to form a layered structure, not an island one. As these materials at the interface remained in existence even after annealing, the distribution of Cu and Si after annealing would be governed by that just after sputtering. The segregation behavior of Cu in the AlCu/TiN structure was the same as that of AlSiCu/TiN.

Chemical Indexing:

AlSiCu-TiN int - AlSiCu int - TiN int - Al int - Cu int - Si int - Ti int - N int - AlSiCu ss - Al ss - Cu ss - Si ss - TiN bin - Ti bin - N bin (Elements - 3,2,5)

Copyright 1996, IEE

4/3,AB,CI/7

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

5102365 INSPEC Abstract Number: B9512-2550F-037

**Title: Diffusion in several materials relevant to Cu interconnection technology**

Author(s): Gupta, D.

Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA

Journal: Materials Chemistry and Physics vol.41, no.3 p.199-205

Publication Date: Aug. 1995 Country of Publication: Switzerland

CODEN: MCHPDR ISSN: 0254-0584

U.S. Copyright Clearance Center Code: 0254-0584/95/\$09.50

Language: English

Abstract: Knowledge of copper diffusion in conducting, dielectric and diffusion barrier thin films relevant to the upcoming Cu interconnection technology is important in order to understand electromigration and prevent degradation of the active devices in Si. Copper diffusion in several thin films considered essential for substitution of Al with Cu interconnects to reduce RC delays is discussed, and the available data are compiled. Fast diffusion of Cu has been observed through inorganic and organic dielectric films, so that the conducting Cu films will require encapsulation. Diffusion of Cu through CVD-W, TiAl/sub 3/-0.5%Cu, TiCu and beta-Ta diffusion barriers has also been studied in a comparative manner.

Chemical Indexing:

W int - W el (Elements - 1)

Ta int - Ta el (Elements - 1)

TiAlCu int - Al int - Cu int - Ti int - TiAlCu ss - Al ss - Cu

Rest pages I delivered  
05/1/00 AB

?show files; ds

File 2:INSPEC 1969-2000/Mar W4  
(c) 2000 Institution of Electrical Engineers  
File 8:Ei Compendex(R) 1970-2000/Apr W2  
(c) 2000 Engineering Info. Inc.  
File 62:SPIN(R) 1975-2000/Mar W3  
(c) 2000 American Institute of Physics  
File 144:Pascal 1973-2000/Mar  
(c) 2000 INIST/CNRS  
File 9:Business & Industry(R) Jul/1994-2000/May 02  
(c) 2000 Resp. DB Svcs.  
File 16:Gale Group PROMT(R) 1990-2000/May 01  
(c) 2000 The Gale Group  
File 35:DISSERTATION ABSTRACTS ONLINE 1861-1999/DEC  
(c) 2000 UMI

Set	Items	Description
S1	20	(AL-CU-TI OR (ALUMINUM (3N) TITANIUM (3N) COPPER) ) AND IN- TERCONNECT? AND (ELECTROMIGR? OR ELECTRO()MIGR?)
S2	17	REMOVE DUPLICATES (unique items)

2/3,AB/15 (Item 2 fr m file: 35)  
DIALOG(R)File 35:DISSERTATION ABSTRACTS ONLINE  
(c) 2000 UMI. All rts. reserv.

01473622 AADAAI9609017

**STRESS AND CURRENT-INDUCED PHENOMENA IN THIN, CONSTRAINED METALLIZATIONS  
(ELECTRICAL INTERCONNECTS, ALUMINUM, COPPER, TITANIUM ALUMINIDE)**

Author: BROWN, DIRK DEWAR

Degree: PH.D.

Year: 1996

Corporate Source/Institution: CORNELL UNIVERSITY (0058)

Source: VOLUME 56/12-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 6986. 443 PAGES

Thin, constrained metallizations are used as **interconnects** in microelectronic systems. The reliability of these metallizations can be drastically affected by stress and current-induced phenomena. In this dissertation, new experimental and theoretical work is presented that extends the current understanding of stress and current effects on thin, constrained metallizations from the point of view of **interconnect** reliability.

Two specific metallizations are addressed in detail: (i) narrow, passivated metal lines used as **interconnects** in integrated circuits, and (ii) copper-plated through-holes used to connect different levels of metallization within a printed circuit board and to connect chip-carriers to a board.

Three phenomena are treated for narrow, passivated metal lines: stress-induced voiding, the formation of intermetallics, and **electromigration** -induced voiding.

In the treatment of stress-induced voiding, new modeling and experimental results are presented on void growth resulting from thermally-induced stresses in narrow, passivated Al-alloy and Cu lines. Thermally-induced stresses are stresses which arise from a thermal expansion mismatch between the metal and its surroundings during thermal excursions. In the treatment of intermetallic formation, experimental results are presented on Kirkendall voiding in passivated Al-alloy lines, and on stresses associated with  $\text{TiAl}_3$  formation in Ti/Al-alloy thin film stacks. Finally, in the treatment of **electromigration** -induced voiding, physically based statistical models are presented for **electromigration** -induced damage in narrow, passivated lines. These models are shown to correlate well with both void growth data and failure distribution data. Based on these models, **electromigration** data can be extrapolated to various conditions of stress, current, and temperature, as well as to early cumulative failure regimes not easily accessible experimentally.

The ductile fracture of copper-plated through-holes is also treated in this dissertation. During thermal excursions, very high stresses can be formed in the Cu plating of a plated through-hole due to a mismatch in the thermal coefficient of expansion with the printed circuit board. These stresses can cause cracks in the Cu, resulting in the failure of the plated through-hole. Experimental and theoretical results are presented on fracture mechanisms in copper-plated through-holes, and suggestions are made for material improvement and testing.

2/3,AB/16 (Item 3 from file: 35)  
DIALOG(R)File 35:DISSERTATION ABSTRACTS ONLINE  
(c) 2000 UMI. All rts. reserv.

01212773 AAD9209852

**ROLES OF TITANIUM-INTERMETALLIC COMPOUND LAYER(S) ON THE ELECTROMIGRATION  
RESISTANCE OF ALUMINUM- COPPER INTERCONNECTING STRIPES ( ALUMINUM-  
COPPER, TITANIUM, INTERMETALLIC COMPOUND LAYERS)**

Author: LEE, CHII-CHANG

Degree: ENG.SC.D.

Year: 1991

Corporate Source/Institution: COLUMBIA UNIVERSITY (0054)

Source: VOLUME 52/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 6028. 167 PAGES

Four different configurations have been tested: Al-Cu, Ti/Al-Cu, Al-Cu/Ti, and Ti/Al-Cu/Ti to evaluate the possible contributions of Ti-intermetallic compound layer(s) to enhancement of the lifetime to failure. Basically, the proposed mechanisms can be classified into two groups: shunting effect and effects limited to changes in Al-Cu conducting layer(s). A resistance monitoring technique was adopted to supplement lifetime measurement to separate these two effects. By correlating the first resistance jump (spike) to the happening of a complete open across Al-Cu layer, it was found that the shunting effect contributes to enhancement of the lifetime by 4 times in Ti/Al-Cu, 2 times in Al-Cu/Ti, and 2 times in Ti/Al-Cu/Ti. A Ti underlayer was found to contribute mainly the shunting effect. However, from drift velocity measurements and failure mode analysis, it is possible to deduce that a Ti overlayer contributes not only the shunting effect but also another effect that acts to diminish the grain boundary mass transport rate by a factor of about 76. It is believed that the latter effect is a consequence of the high compressive yield strength conferred by the Ti-intermetallic compound overlayer to the Al-Cu layer.

Finally, an important non-destructive technique, based on the characteristic x-rays generated by energetic electrons, to characterize the mass divergences in multilayer **interconnects**, was developed in this research, called SMEISIS, representing Simultaneous Multiple Elements Intensity Scanning of **Interconnecting** Stripes. This technique was proved to be capable of revealing detail about the shapes, nature, and location of mass divergence that cannot be revealed by thermal wave image technique and that requires time consuming multiple sectioning in TEM and SEM methods.

2/3,AB/17 (Item 4 from file: 35)

DIALOG(R) File 35:DISSERTATION ABSTRACTS ONLINE

(c) 2000 UMI. All rts. reserv.

1017385 AAD8815003

**LAYERED AND HOMOGENEOUS ALUMINUM ALLOYS FOR INTERCONNECTION DEVICES IN INTEGRATED CIRCUITS**

Author: GARDNER, DONALD STANLEY

Degree: PH.D

Year: 1988

Corporate Source/Institution: STANFORD UNIVERSITY (0212)

Source: VOLUME 49/06-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 2310. 387 PAGES

Aluminum has been applied for **interconnections** in integrated circuits since their invention because of its low resistivity and silicon compatibility; however, with the scaling of integrated circuits, pure aluminum has become unsuitable. Aluminum alloyed with copper and silicon reduces the problems of **electromigration**, hillock growth, and junction spiking but, because of continued size reductions, such alloying is also becoming less effective.

The synthesis of films via sputtering facilitates the deposition of many materials in one process cycle. This approach was used to fabricate a multilayered metal structure for a single level of **interconnection**. When these structures are fabricated with aluminum-silicon and titanium, failures such as interlevel shorts and **electromigration** are reduced and **interconnection** resistivity remains low which is important for maximum performance in micron and submicron integrated circuits. **Interconnections** are treated as if they are a device that can be designed to reliably perform a function in the analyses presented.

Because interlevel failures are caused by stresses that develop in the aluminum films during high-temperature processing, mechanical stresses are examined by means of a highly sensitive laser-based measurement apparatus.

Stress as a function of temperature is measured for several alloys and layered films consisting of **aluminum** with silicon, **copper** , **titanium** , tantalum, vanadium, tungsten, and/or titanium silicide. Several variations in the film stress of these alloys during thermal cycling are observed, and models are proposed to explain these results.

Scaling theory for **interconnection** resistivity and **electromigration** is also developed and used to formulate guidelines. Recent **electromigration** results are then compared to theoretical predictions.

=> t 138 std abs hit

L38 ANSWER 1 OF 5 CAPLUS COPYRIGHT 2000 ACS

AN 1999:165409 CAPLUS

DN 130:289620

TI Formation of electrical contact through an Alodine coating

AU Wehr, Anna; Hardee, Harry C.; Aukland, Neil R.; Klavens, David

CS Advanced Interconnections Laboratory, New Mexico State University, Las Cruces, NM, 88003-8001, USA

SO Proc. - Electron. Compon. Technol. Conf. (1998), 48th, 14-20  
CODEN: PETCES

PB Institute of Electrical and Electronics Engineers

DT Journal

LA English

AB In some airplane applications, Cd plated connectors are mounted to Alodine

coated Al brackets. Good elec. bonding or grounding is essential through the resistive Alodine coating. The Alodine film is a chromate conversion coating applied to protect Al against corrosion. A great deal of variability and increase with time is characteristic for the contact resistance at the interface between the Cd-plated connector and bracket. Significant rework is sometimes required to stabilize the bond. An understanding of the phenomena responsible for the value of the contact resistance between a Cd-plated connector and an Alodine coated bracket

was

the goal of this research work. In this research work, SEM and Energy-Dispersive x-ray Anal. (EDX) were used to examine the microstructure of virgin Alodine coatings on unassembled brackets. The next set of SEM and EDX exams. was conducted on Alodine coated brackets that had been assembled and disassembled with a connector.

CC 76-2 (Electric Phenomena)

Section cross-reference(s): 56, 66

IT 7429-90-5, Aluminum, processes 7440-43-9, Cadmium, processes  
51433-91-1, Alodine 600 125352-58-1, 6013 T4

RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)  
(formation of elec. contact through Alodine coating)

=> t 138 3 std abs hit

L38 ANSWER 3 OF 5 CAPLUS COPYRIGHT 2000 ACS

AN 1994:593500 CAPLUS

DN 121:193500

TI Forming a layer, especially in semiconductor wafer processing

IN Dobson, Christopher David

PA Electrotech Ltd., UK

SO PCT Int. Appl., 30 pp.

CODEN: PIXXD2

DT Patent

LA English

IC ICM H01L

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9413008	A2	19940609	WO 1993-GB2359	19931116
	WO 9413008	A3	19940721		

W: GB, JP, KR, US  
 RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE  
 JP 07503106 T2 19950330 JP 1993-512877 19931116  
 PRAI GB 1992-24260 19921119  
 WO 1993-GB2359 19931116  
 AB The method comprises depositing a layer of a material on the surface of  
 an article such that the layer covers the mouth of a recess leaving a void  
 below the closed mouth. Without elevating their temp., the article and  
 layer are then subjected to sufficient elevated pressures (e.g.,  
 pressurized liq.) to cause the layer to deform into the recess.  
 Magnetron sputtering is used in the method and heating the article increases the  
 mobility of the deposited material. Also provided is app. for use in  
 carrying out these methods, which are of particular use in the processing  
 of semiconductor wafers.  
 CC 76-3 (Electric Phenomena)  
 Section cross-reference(s): 75  
 IT 7429-90-5, Aluminum, uses 157905-76-5, Aluminum 92-100, copper  
 0-4, silicon 0-2, titanium 0-2  
 RL: PEP (Physical, engineering or chemical process); PROC (Process)  
 (deposition of, in processing of semiconductor wafers)



=> s 125352-58-1/rn

L39 1 125352-58-1/RN

=> d scan

L39 1 ANSWERS REGISTRY COPYRIGHT 2000 ACS

IN Aluminum alloy, base, Al 95-98, Mg 0.8-1.2, Cu 0.6-1.1, Si 0.6-1.0, Mn  
0.20-0.8, Fe 0-0.50, Zn 0-0.25, Cr 0-0.10, Ti 0-0.10 (AA 6013) (9CI)

MF Al . Cr . Cu . Fe . Mg . Mn . Si . Ti . Zn

CI AYS

Component	Component Percent	
=====+=====		
Al	95	- 98
Mg	0.8	- 1.2
Cu	0.6	- 1.1
Si	0.6	- 1.0
Mn	0.20	- 0.8
Fe	0	- 0.50
Zn	0	- 0.25
Cr	0	- 0.10
Ti	0	- 0.10

Al Ti Cu

Si

Ti

Recalculation of atomic percent composition to weight percent composition

Al- Cu Ti 99.4[at%] Al : 0.5 [at%] Cu: 0.1[at%]Ti

**In this composition**

“Molecular” weight of composition

$$26.98 \times 0.994 + 63.54 \times 0.005 + 47.9 \times 0.001 = 26.818 + 0.317 + 0.479 = 27.614$$

Weight composition of elements (wt%)

$$\text{Al} \quad 26.818 / 27.614 = 97.12 \text{ [wt\%]} \sim 97 \text{ [wt\%]}$$

$$\text{Cu} \quad 0.317 / 27.614 = 1.14 \text{ [wt\%]} \sim 1.1 \text{ [wt\%]}$$

$$\text{Ti} \quad 0.479 / 27.614 = 0.17 \text{ [wt\%]} \sim 0.2 \text{ [wt\%]}$$

ss - Ti ss (Elements - 3)  
Cu int - Cu el (Elements - 1)  
Copyright 1995, FIZ Karlsruhe

4/3,AB,CI/8

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

5093412 INSPEC Abstract Number: B9512-2550F-012

**Title: Enhanced EM endurance of TiN/AlCu/TiN/sub x/ interconnection**

Author(s): Jeong Soo Byun; Jun Ki Kim; Kwan Goo Rha; Woo Shik Kim

Author Affiliation: Semicond. Res. Lab., GoldStar Electron Co. Ltd., Cheongju, South Korea

Conference Title: 1994 International Integrated Reliability Workshop Final Report (Cat. No.94TH0654-4) p.144

Publisher: IEEE, New York, NY, USA

Publication Date: 1994 Country of Publication: USA v+155 pp.

ISBN: 0 7803 1908 7

U.S. Copyright Clearance Center Code: 0 7803 1908 7/94/\$4.00

Conference Title: Proceedings of 1994 IEEE International Integrated Reliability Workshop (IRWS)

Conference Sponsor: IEEE Electron Devices Soc.; IEEE Reliability Soc

Conference Date: 16-19 Oct. 1994 Conference Location: Lake Tahoe, CA, USA

Language: English

Abstract: Summary form only given. In submicron devices, TiN is used as a barrier layer in multilayered aluminum **interconnection** (e.g., TiN/Al/TiN). The conventional TiN layer is formed by reactive sputtering, which shows a columnar grain structure about the size of 10 nm. In this study, we focused on another technique of forming TiN from TiN/sub x/, and compared the electromigration (EM) endurance of the multilayered interconnections using TiN/sub x/ and conventional TiN. In order to investigate the structural aspects of aluminum and the TiN formed from the TiN/sub x/ layer, the samples were prepared as follows. TiN/sub x/ film of 50 nm thickness was reactively deposited on the oxidized (400 nm thick) silicon wafer by using DC magnetron sputtering in a mixed gas atmosphere of argon and nitrogen, in which the volume percent of nitrogen was fixed at 15%. After thermal treatment at 600 degrees C for 20 sec using RTA, Al-0.5%Cu film (500 nm thick) and TiN (40 nm thick) film were sequentially deposited. After patterning of aluminum stripes of 0.4 mu m width and 1400 mu m length, the samples were alloyed at 400 degrees C, 30 min in 15% H/sub 2//N/sub 2/ ambient. Finally, a passivation layer consisting of CVD nitride (1.2 mu m thick) and CVD oxide (0.4 mu m thick) was deposited. The film properties before and after RTA were analyzed using RBS, XRD, and AES. Such an **interconnection** showed extremely high EM endurance (MTTF approximately 10/sup 4/ min) in comparison with that using the conventional TiN as an underlying barrier layer (MTTF approximately 10/sup 2/ min). It is suggested that the crystal continuity between the Al and the TiN suppresses interface and grain boundary diffusion of Al atoms to improve the EM endurance.

Chemical Indexing:

TiN-AlCu-TiN int - AlCu int - TiN int - **Al** int - **Cu** int - **Ti** int -  
N int - AlCu bin - TiN bin - **Al** bin - **Cu** bin - **Ti** bin - N bin  
(Elements - 2,2,2,4)

Copyright 1995, IEE

4/3,AB,CI/15

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

04358677 INSPEC Abstract Number: B9304-2550F-019

**Title: A quarter-micron interconnection technology using Al-Si-Cu/TiN alternated layers**

Author(s): Kikkawa, T.; Aoki, H.; Ikawa, E.; Drynan, J.

Author Affiliation: NEC Corp., Sagami City, Japan  
Conference Title: International Electron Devices Meeting 1991. Technical  
Digest (Cat. No.91CH3075-9) p.281-4  
Publisher: IEEE, New York, NY, USA  
Publication Date: 1991 Country of Publication: USA 977 pp.  
ISBN: 0 7803 0243 5  
U.S. Copyright Clearance Center Code: CH3075-9/91/0000-0281\$1.00  
Conference Sponsor: IEEE  
Conference Date: 8-11 Dec. 1991 Conference Location: Washington, DC,  
USA

Language: English

Abstract: A novel **interconnection** structure using Al-Si-Cu/TiN alternated layers has been investigated as a quarter-micron **interconnection** candidate for 256 MDRAM. A TiN/Al-1%Si-0.5%Cu/TiN/Al-1%Si-0.5%Cu/TiN/Ti layered film structure was designed for both electro- and stress-migration-resistant interconnections. This alternated layer structure has extremely high endurance in terms of mechanical hardness, tensile strength, and electromigration lifetime.

Chemical Indexing:

AlSiCu-TiN int - AlSiCu int - TiN int - **Al** int - **Cu** int - Si int -  
**Ti** int - N int - AlSiCu ss - **Al** ss - **Cu** ss - Si ss - TiN bin - **Ti**  
bin - N bin (Elements - 3,2,5)  
AlSiCu ss - Al ss - Cu ss - Si ss (Elements - 3)

**4/3,AB,CI/18**

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

04047297 INSPEC Abstract Number: B9201-2550F-029

**Title: Passivation effects on step AlCu/TiN line electromigration performance**

Author(s): Ferlazzo, L.; Lormand, G.; Reimbold, G.

Author Affiliation: D.LETI CENG, Grenoble, France

Journal: Microelectronic Engineering vol.15, no.1-4 p.487-90

Publication Date: Oct. 1991 Country of Publication: Netherlands

CODEN: MIENEF ISSN: 0167-9317

U.S. Copyright Clearance Center Code: 0167-9317/91/\$03.50

Conference Title: ESSDERC '91: 21st European Solid State Device Research  
Conference

Conference Sponsor: Ecole Polytechnique Federale, Lausanne; ASCOM; IBM;  
IEEE; et al

Conference Date: 16-19 Sept. 1991 Conference Location: Montreux,  
Switzerland

Language: English

Abstract: Electromigration performance of AlCu/TiN with topography lines has been investigated and the results show a dependence of their behaviour on overlayer. When cross section reduction alone nearly accounts for the lifetime decrease of uncoated samples relative to a flat structure, it is insufficient to account for coated samples. The simulations that were performed indicate that thermal gradients along the line are not important. Different microstructural fluctuations for both cases may be considered as supported by grain size analysis.

Chemical Indexing:

AlCu-TiN int - AlCu int - TiN int - **Al** int - **Cu** int - **Ti** int - N  
int - AlCu bin - TiN bin - **Al** bin - **Cu** bin - **Ti** bin - N bin (Elements  
- 2,2,4)

**4/3,AB,CI/19**

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

04023965 INSPEC Abstract Number: B91076944

**Title: A study of AlCu (1%) sputter deposition parameters on electromigration**

Author(s): Bordelon, M.; Shlepr, M.; Jones, K.  
Author Affiliation: Harris Semicond., Melbourne, FL, USA  
Conference Title: 1991 Proceedings. Eighth International IEEE VLSI  
Multilevel Interconnection Conference (Cat. No.91TH0359-0) p.402-4  
Publisher: IEEE, New York, NY, USA  
Publication Date: 1991 Country of Publication: USA 456 pp.  
ISBN: 0 87942 673 X  
U.S. Copyright Clearance Center Code: TH0359-0/91/0000-0402\$01.00  
Conference Sponsor: IEEE  
Conference Date: 11-12 June 1991 Conference Location: Santa Clara, CA,  
USA

Language: English

Abstract: This work investigates the impact of deposition parameters on thin film quality of an AlCu/TiW metallization system. A statistically designed experiment was conducted to study aluminum deposition temperature, pressure, power, and underlying dielectric stress. Determination of Median Time to Failure (MTF) by electromigration stress was used to determine the optimum deposition parameters. Data on microstructure, as characterized by TEM and resistivity ratio (RR) measurements made on patterned conductors, are compared to the observed MTF's. Substrate temperature during deposition was found to have the most significant impact on electromigration. No correlation of MTF to RR measurements was observed. The improved EM performance at low temperature is believed to be due to a more uniform distribution and a larger number of (-)-Al/sub 2/Cu precipitates.

Chemical Indexing:

AlCu-TiW int - AlCu int - TiW int - **Al** int - **Cu** int - **Ti** int - W  
int - AlCu bin - TiW bin - **Al** bin - **Cu** bin - **Ti** bin - W bin (Elements  
- 2,2,4)  
Al2Cu int - Al2 int - Al int - Cu int - Al2Cu bin - Al2 bin - Al bin - Cu  
bin (Elements - 2)

4/3,AB,CI/20

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

04023963 INSPEC Abstract Number: B91076942

**Title: Effect of nitrogen containing underlayers on aluminum electromigration**

Author(s): Jain, V.; Pramanik, D.  
Author Affiliation: VLSI Technol. Inc., San Jose, CA, USA  
Conference Title: 1991 Proceedings. Eighth International IEEE VLSI  
Multilevel Interconnection Conference (Cat. No.91TH0359-0) p.396-8  
Publisher: IEEE, New York, NY, USA  
Publication Date: 1991 Country of Publication: USA 456 pp.  
ISBN: 0 87942 673 X  
U.S. Copyright Clearance Center Code: TH0359-0/91/0000-0396\$01.00  
Conference Sponsor: IEEE  
Conference Date: 11-12 June 1991 Conference Location: Santa Clara, CA,  
USA

Language: English

Abstract: Electromigration performance of Al-1% Cu films deposited on TiW underlayer have been studied. Role of nitrogen impurity in the underlying TiW film on electromigration has been investigated. The study shows that increasing nitrogen content in the underlayer results in worse electromigration performance.

Chemical Indexing:

AlCu bin - Al bin - Cu bin (Elements - 2)  
AlCu-TiW:N int - TiW:N int - AlCu int - TiW int - **Al** int - **Cu** int -  
**Ti** int - N int - W int - TiW:N ss - **Ti** ss - N ss - W ss - AlCu bin - TiW  
bin - **Al** bin - **Cu** bin - **Ti** bin - W bin - N el - N dop (Elements -  
2,2,1,3,5)  
TiW sur - Ti sur - W sur - TiW bin - Ti bin - W bin (Elements - 2)

4/3,AB,CI/21

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

04023926 INSPEC Abstract Number: B91076906

**Title: Electromigration improvements with titanium underlay and overlay in Al(Cu) metallurgy**

Author(s): Estabil, J.J.; Rathore, H.S.; Levine, E.N.

Author Affiliation: Gen. Technol. Div., IBM Corp., Hopewell Junction, NY, USA

Conference Title: 1991 Proceedings. Eighth International IEEE VLSI Multilevel Interconnection Conference (Cat. No.91TH0359-0) p.242-8

Publisher: IEEE, New York, NY, USA

Publication Date: 1991 Country of Publication: USA 456 pp.

ISBN: 0 87942 673 X

U.S. Copyright Clearance Center Code: TH0359-0/91/0000-0242\$01.00

Conference Sponsor: IEEE

Conference Date: 11-12 June 1991 Conference Location: Santa Clara, CA, USA

Language: English

Abstract: The reliability advantages of Ti-Al(Cu)-Ti are introduced in this work. Outstanding tolerance to electromigration damage is measured both single level interconnections and two-level interconnections with tungsten via-studs. A greater than 100\* improvement in the median time to failure ( $t_{sub 50}$ ) is measured for Ti-Al(Cu)-Ti interconnections over simple Al(Cu). An integrated, four-level metallization has been realized.

Chemical Indexing:

Ti -AlCu-Ti int - AlCu int - Al int - Cu int - Ti int - AlCu bin  
- Al bin - Cu bin - Ti el (Elements - 1,2,1,3)

**4/3,AB,CI/26**

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

03756719 INSPEC Abstract Number: B90075983

**Title: Dry etching of TiN/Al(Cu)/Si for very large scale integrated local interconnections**

Author(s): Hu, C.-K.; Mazzeo, N.; Basavaiah, S.; Small, M.B.; Choi, K.W.

Author Affiliation: IBM, Thomas J. Watson Res. Center, Yorktown Heights, NY, USA

Journal: Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films) vol.8, no.3, pt.1 p.1498-502

Publication Date: May-June 1990 Country of Publication: USA

CODEN: JVTAD6 ISSN: 0734-2101

U.S. Copyright Clearance Center Code: 0734-2101/90/031498-05\$01.00

Conference Title: 36th National Symposium of the American Vacuum Society

Conference Date: 23-27 Oct. 1989 Conference Location: Boston, MA, USA

Language: English

Abstract: Patterning Ti/TiN/Ti/Al(2 wt. % Cu)/Si interconnection lines over 700 nm topographic steps in SiO<sub>2</sub> with an angle of 84 degrees is reported using a reactive ion etching. The etching gas is a mixture of BCl<sub>3</sub>/sub 3//Cl<sub>2</sub>/sub 2//N<sub>2</sub>/sub 2//CHCl<sub>3</sub>/sub 3/ and the etching process uses a combination of high and low reactor pressures in a single wafer etching tool. No metal rails along the sidewall of topographic features were detected using an electrical test site. The etched metal profile shows a near vertical metal sidewall with negligible undercut. The metal linewidths are 0.7 to 1.8  $\mu$ m wide with the variation of about 0.1  $\mu$ m near the steps, due to resist linewidth variations over the topographic step. It also demonstrated that the Al(Cu) line can be a good landing pad for contact hole dielectric etching.

Chemical Indexing:

Ti -TiN-Ti -AlCu-Si int - AlCu int - TiN int - Al int - Cu int - Si  
int - Ti int - N int - AlCu bin - TiN bin - Al bin - Cu bin - Ti  
bin - N bin - Si el - Ti el (Elements - 1,2,1,2,1,5)

?t /3,ab,ci/28

**4/3,AB,CI/28**

DIALOG(R)File 2:INSPEC

(c) 2000 Institution of Electrical Engineers. All rts. reserv.

03568994 INSPEC Abstract Number: B90015033

**Title: Comparison of electromigration phenomenon between aluminum interconnection of various multilayered materials**

**Author(s):** Fujii, T.; Okuyama, K.; Moribe, S.; Torii, Y.; Katto, H.; Agatsuma, T.

**Author Affiliation:** Hitachi Ltd., Tokyo, Japan

**Conference Title:** 1989 Proceedings. Sixth International IEEE VLSI Multilevel Interconnection Conference (Cat. No.89TH0259-2) p.477-83

**Publisher:** IEEE, New York, NY, USA

**Publication Date:** 1989 **Country of Publication:** USA 508 pp.

**U.S. Copyright Clearance Center Code:** TH-0259-2/89/0000-0477\$01.00

**Conference Sponsor:** IEEE

**Conference Date:** 12-13 June 1989 **Conference Location:** Santa Clara, CA, USA

**Language:** English

**Abstract:** The electromigration characteristics of a multilayered system were found to be divided into three stages. The mechanism leading to the stages is discussed in terms of the process of microvoid growth during the electromigration stressing and is correlated with the amount of Si precipitation and the size of the grain boundary of Al films, the reaction layer at the interface, and the resistivity of the barrier metal. The experiments were carried out for MoSi, TiN, and TiW film deposited on oxidized Si (100) wafers by sputtering.

**Chemical Indexing:**

MoSi-AlCuSi-MoSi int - AlCuSi int - MoSi int - Al int - Cu int - Mo int - Si int - AlCuSi ss - Al ss - Cu ss - Si ss - MoSi bin - Mo bin - Si bin (Elements - 2,3,2,4)

Si sur - Si el (Elements - 1)

AlCuSi-TiN int - AlCuSi int - TiN int - Al int - Cu int - Si int - Ti int - N int - AlCuSi ss - Al ss - Cu ss - Si ss - TiN bin - Ti bin - N bin (Elements - 3,2,5)

TiW-AlCuSi-TiW int - AlCuSi int - TiW int - Al int - Cu int - Si int - Ti int - W int - AlCuSi ss - Al ss - Cu ss - Si ss - TiW bin - Ti bin - W bin (Elements - 2,3,2,5)